LSI DOCKET NO. 03-0084

CLAIMS:

What is claimed is:

1. A method for observing the state of internal signals during chip testing, comprising:

receiving specific test signals in at least one module in order to form a plurality of test signal groups;

combining the specific test signals received for each test signal group to create the plurality of test signal groups;

identifying specific test signal groups in order to form a plurality of test signal output groups; and

mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups.

2. The method of claim 1 wherein the at least one module includes a plurality of modules.

3. The method of claim 2, further comprising:

concurrently observing test signals for a plurality of modules.

4. The method of claim 3 wherein the plurality of modules includes identical modules.

5. The method of claim 1 wherein combining the specific test signals received for each test signal group to create the plurality of test signal groups is performed by a multiplexer.

6. The method of claim 1 wherein mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups is performed using byte lane mapping logic.

7. An apparatus for observing the state of internal signals during chip testing, comprising:

multiplexing means for combining test signals in a module to create specified test signal groups;

mapping means for mapping specified test signal groups to specified test output groups.

8. A system for observing the state of internal signals during chip testing, comprising:

means for receiving specific test signals in at least one module in order to form a plurality of test signal groups;

means for combining the specific test signals received for each test signal group to create the plurality of test signal groups;

means for identifying specific test signal groups in order to form a plurality of test signal output groups; and

means for mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups.

9. The system of claim 8 wherein the at least one module includes a plurality of modules.

10. The system of claim 9, further comprising:

concurrently observing test signals for a plurality of modules.

11. The system of claim 10 wherein the plurality of modules includes identical modules.

12. The system of claim 8 wherein the means for combining the specific test signals received for each test signal group to create the plurality of test signal groups is a multiplexer.

13. The system of claim 8 wherein the means for mapping the specific test signal groups identified for each test signal output group to create the plurality of test signal output groups is performed using byte lane mapping logic.